

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	615	memory same ((even or odd) near3 address) same (interleav\$3 or alternat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 06:23
L2	14	memory same ((even or odd) near3 address) same (interleav\$3 or alternat\$3) same (control\$4 or arbiter) same select\$3 same enable	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 06:36
L3	27	"711"/\$.ccls. and (write near3 enable) same (read near3 enable) same update	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 06:40
L4	12	"711"/\$.ccls. and (write adj enable) same (read adj enable) same update	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 06:43
L5	31	(write adj enable) same (read adj enable) same (flag or bit or semaphore) same update	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 06:53
L9	23	(write adj enable) with (read adj enable) with (flag or bit or semaphore) same reset	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 07:13
L10	2	(write adj enable) with (read adj enable) with (flag or bit or semaphore) same update	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 07:15
L11	1663	update with address near3 register	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 07:15
L12	47	module same update with address near3 register	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 07:15

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L13	9	"711"/\$.ccls. and module same update with address near3 register	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 07:21
L14	356	"711"/\$.ccls. and update with address near3 register	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 07:22
L15	20464	"711"/\$.ccls. and update with (read adj address) or (write adj address)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 07:22
L16	95	"711"/\$.ccls. and update with ((read adj address) or (write adj address))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 07:22
S1	2	(FIFO or first-in-first-out or (first adj in adj first adj out)) with ((single or one) near3 port) same (even or odd) near3 address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/19 21:49
S2	10	("20030034797" "5084841" "5471583" "5663910" "5974482").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/19 21:41
S3	0	("2005/0091465").URPN.	USPAT	OR	ON	2006/03/19 21:48
S4	13	(FIFO or first-in-first-out or (first adj in adj first adj out)) same (even or odd) near3 address same alternat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/19 21:55
S5	13	(FIFO or first-in-first-out or (first adj in adj first adj out)) same (even or odd) near3 address same interleav\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/20 06:11
S6	0	711/005.ccls. and (even or odd) near3 address same (interleav\$3 or alternat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/20 06:12

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S7	45	711/5.ccls. and (even or odd) near3 address same (interleav\$3 or alternat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 06:22
S8	28	711/5.ccls. and (even or odd) near3 address with (interleav\$3 or alternat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/20 06:19
S9	2	711/150.ccls. and (even or odd) near3 address with (interleav\$3 or alternat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/20 06:20
S10	3	711/151.ccls. and (even or odd) near3 address with (interleav\$3 or alternat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/20 06:20
S11	22	711/167.ccls. and (even or odd) near3 address with (interleav\$3 or alternat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/20 06:22
S12	6	711/168.ccls. and (even or odd) near3 address with (interleav\$3 or alternat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/20 06:23
S13	7	711/169.ccls. and (even or odd) near3 address with (interleav\$3 or alternat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/20 06:23

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**PALM INTRANET**

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L1	1	(Fifo same (even adj address) same (odd adj address) same (select\$3 or pick\$3 or elect\$3 or choos\$3) same (write adj enable) same (read adj enable) same (address near3 update)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 08:18
L3	1	(Fifo same (select\$3 or pick\$3 or elect\$3 or choos\$3) same (write adj enable) same (read adj enable) same (address near3 update)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 08:18
L4	1	(memory same (select\$3 or pick\$3 or elect\$3 or choos\$3) same (write adj enable) same (read adj enable) same (address near3 update)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 08:19
L5	0	(buffer same (select\$3 or pick\$3 or elect\$3 or choos\$3) same (write adj enable) same (read adj enable) same (address near3 update)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 08:19
L6	1	((select\$3 or pick\$3 or elect\$3 or choos\$3) same (write adj enable) same (read adj enable) same (address near3 update)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/29 08:19

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[FPGA prototype queuing module for high performance ATM switching - group of 5 »](#)

H Duan, JW Lockwood, SM Kang - ASIC Conference and Exhibit, 1994. Proceedings., Seventh ..., 1994 - [ieeexplore.ieee.org](#)

... generates read signals to the external **FIFO** memory ... bus must be stable before the **read enable** signal is ... is used to handle lookup table **update** operation, which ...

Cited by 7 - [Related Articles](#) - [Web Search](#)

[Efficient Modeling of Embedded Memories in Bounded Model Checking - group of 2 »](#)

M Ganai, A Gupta, P Ashar - Proceedings of CAV, 2004 - Springer

... several forms such as RAM, stack, and **FIFO** with at ... j, **write enable** is active at j, **read enable** is active ... i =EMM\_Constraints(i,C i-1 );//update the constraints ...

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[The Central Trigger Processor Monitoring module \(CTP\\_MON\) in the ATLAS Level-1 Trigger System](#)

N Ellis, P Farthouat, P Gallno, G Schuler, R ... - memory - [lhcc-electronics-workshop.web.cern.ch](#)

... Trigger sub-systems at 40 MHz **update** rate, corresponding ... 2: Timing parameters for the IDT **FIFO** The simulation ... Setup time for **read enable** 3.0 ns (min) - 6.3 ns ...

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[Scaling and performance of a priority packet queue for real-time applications - group of 2 »](#)

D Picker, RD Fellman - Real-Time Systems Symposium, 1994., Proceedings., 1994 - [ieeexplore.ieee.org](#)

... The Packet **FIFO** has the same segmented architecture as the PPQ, but does ... Page 4 Signal

Description Width '1 W **Write Enable** - Asserted during insertion of a ...

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[An Executable Operational Semantics for SystemC using Abstract State Machines - group of 2 »](#)

A Gawanmeh, A Habibi, S Tahar - [hvg.ece.concordia.ca](#)

... where we can not explicitly declare the calling process to be sensitive to the **FIFO** ... popped out of channel, and the channel is scheduled for **update** at the ...

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[An implementation of a residential gateway controller for a fixed bandwidth-sharing multiservices ...](#)

T Ji, S Song, L Wei - Electrical and Computer Engineering, 2004. Canadian ..., 2004 - [ieeexplore.ieee.org](#)

... or first-in first-out (**FIFO**) functions. ... Therefore, **read enable** signal was generated separately with STS ... The FSAN VDSL Working Group - Update," Third Workshop ...

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[Differential register bank design for self timed differential bipolar technology -](#)

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[Virtual Memory Mapped Network Interface for the SHRIMP Multicomputer - group of 7 »](#)

MA Blumrich, K Li, R Alpert, C Dubnicki, EW Felten ... - portal.acm.org

... The network interface supports two transfer strate- gies: automatic **update** and deliberate **update**. Under automatic **update**, a sending process can map the ...

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[Domain-specific high-level modeling and synthesis for ATM switch design using VHDL - group of 6 »](#)

MTC Lee, YC Hsu, B Chen, M Fujita - Proceedings of the 33rd annual conference on Design ... , 1996 - portal.acm.org

... of the cell, this address is kept in a **Read Address FIFO** RAF0 or ... components operating concurrently for the highways to access and **update** the cell **FIFO**, ad- ...

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[\[pvs\] High-Level Design and Validation of ATM Switch](#)

S Rajan, M Fujita, K Yuan, M Lee - Proc. IEEE International High Level Design Validation and ... - pvs.csl.sri.com

... WAF, RAF, WC, and RC, correctly **update** the shared ... that every RAF unit behaves like a **FIFO** queue, and ... 3.3 (RC Liveness) AF(output port **read address** = RAF(RAF ...

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[A flexible broadband packet switch for a multimedia integratednetwork](#)

CB Woodworth, MJ Karol, RD Gitlin - Communications, 1991. ICC 91, Conference Record. IEEE ... , 1991 - ieeexplore.ieee.org

... Note that the **update** lines and control logic can operate ... reasons: (i) RAMs are more dense than **FIFO** chips; (ii ... the N RAMs with a common **read address** pointer and ...

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[A Parametric Design of a Built-in Self-Test FIFO Embedded Memory - group of 6 »](#)

S Barbagallo, F Fumini, D Sciuto - ieeexplore.ieee.org

... the architecture of the **FIFO** memory chosen is ... phases: request acquisition, memory enable and counter **update**. ... the same writing order, the **read address** can never ...

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[Design of the AlphaServer Multiprocessor Server Systems - group of 6 »](#)

FM Hayes - Digital Technical Journal, 1994 - public.planetmirror.com

Page 1. The AlphaServer 2100 (large pedestal) and the AlphaServer 2000 (small pedestal) servers from Digital combine multiprocessing ...

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[ATM switch design by high-level modeling, formal verification and high-level synthesi](#)

SP Rajan, M Fujita, K Yuan, MTC Lee - ACM Transactions on Design Automation of Electronic Systems ... , 1998 - portal.acm.org

... cell TAGs to one of the two **Read-Address-FIFOs**: RAF0 ... At power-on or reset, the **Write-Address FIFO** (WAF) unit ... WAF, RAF, WC, and RC, correctly **update** the shared ...

MR